TQMaX4XxL
User's Manual

TQMaX4XxL UM 0100
11.04.2024

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	11.04.2024	Kreuzer	All	Initial release

1. ABOUT THIS MANUAL

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive devices and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMaX4XxL and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you power up the TQMaX4XxL or the Starterkit, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manuals of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBaX4XxL circuit diagram
- MBaX4XxL User's Manual
- Sitara™ AM6442 / AM2434 Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqmax4xxl

2. BRIEF DESCRIPTION

The TQMaX4XxL is a universal TQ-LGA mini module based on the TI Sitara family AM64x and AM243x processors with ARM Cortex A53, Cortex R5 and Cortex M4 cores.

This User's Manual describes the hardware of the TQMaX4XxL Rev.020x and refers to some software settings.
It does not replace the AM6442 / AM2434 Reference Manual (3).

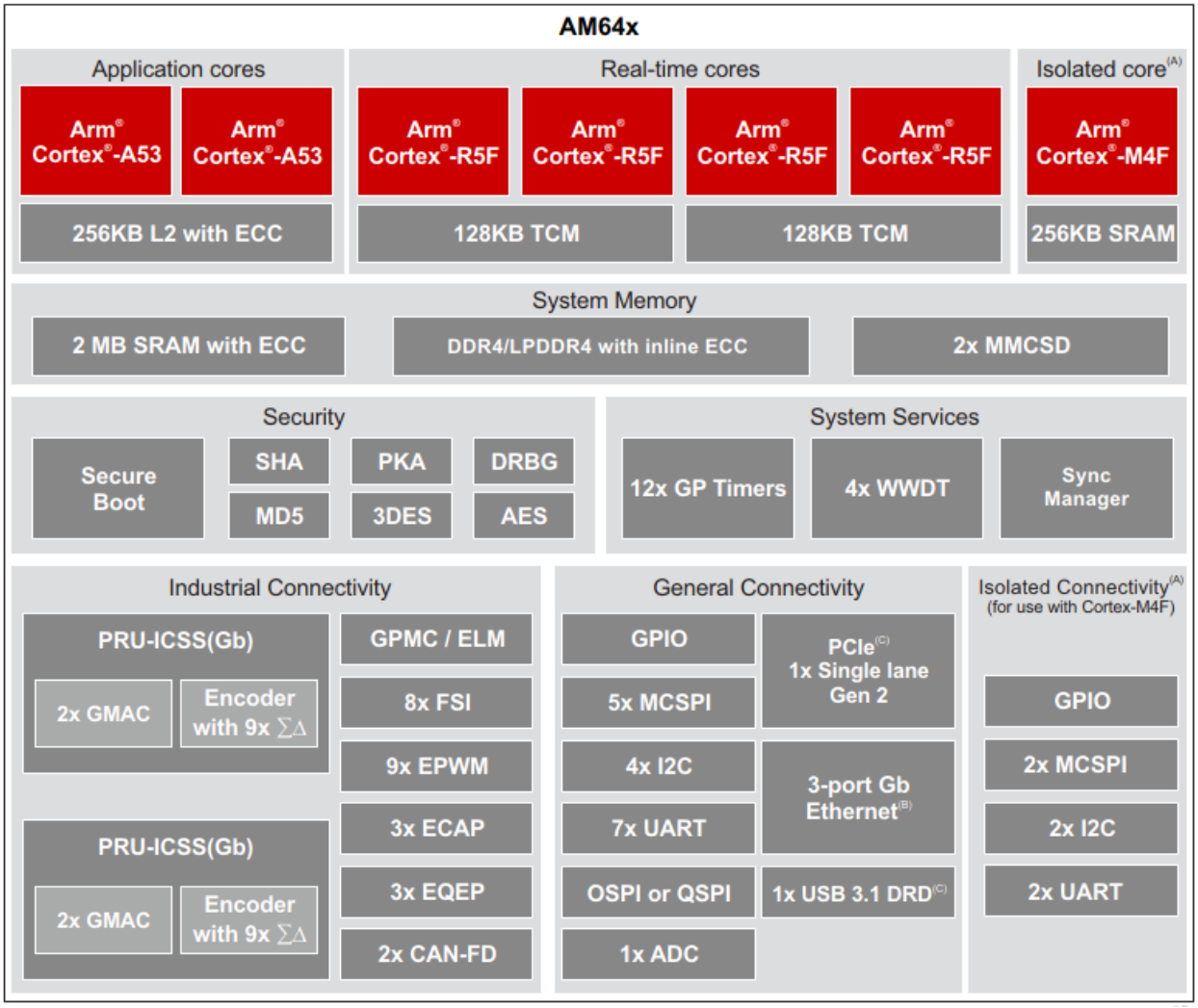

Figure 1: Block diagram AM6442
(Source: Texas Instruments)

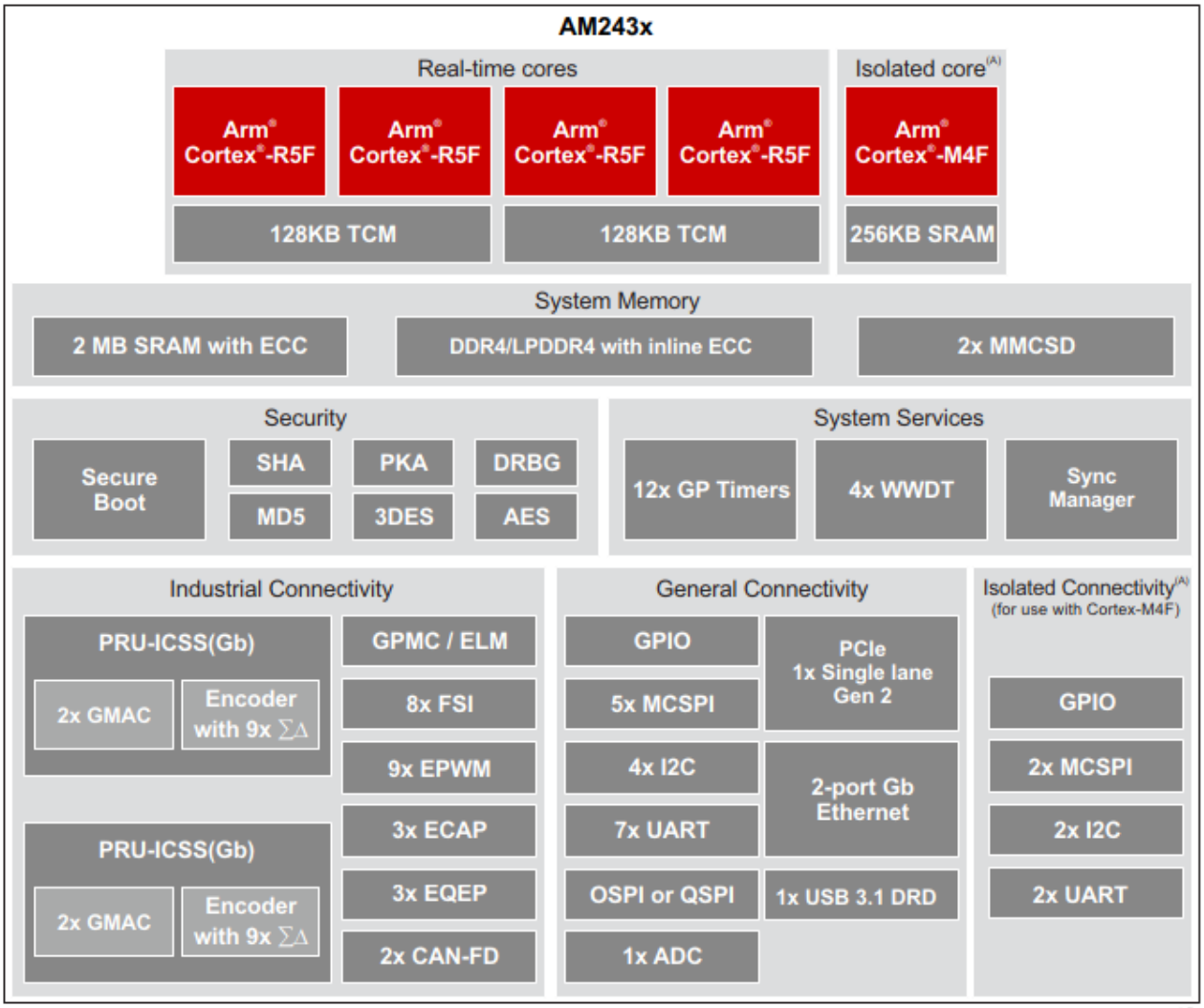

Figure 2: Block diagram AM243x

(Source: Texas Instruments)

All useful AM64x / AM243x signals are routed to the TQMaX4XxL pads. There are no restrictions for customers using the TQMaX4XxL with respect to an integrated customised design.

Please take note of that not all interfaces can be used simultaneously.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMaX4XxL, and the BSP provided by TQ-Systems GmbH, see also section 4.

3.1 System overview

3.1.1 System architecture / block diagram

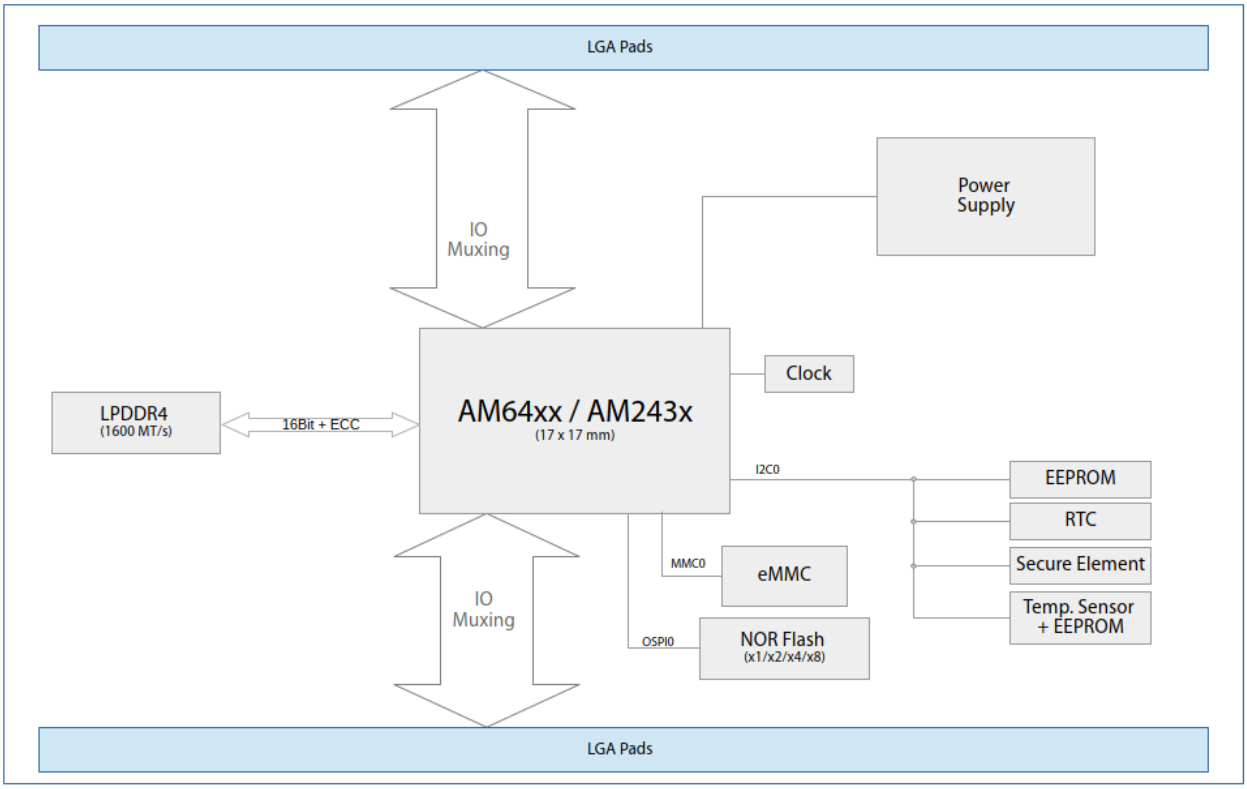

Figure 3: Block diagram TQMaX4XxL

3.1.2 Functionality

The following key functions are implemented on the TQMaX4XxL:

- AM64x, AM243x CPU
- 16-bit LPDDR4 memory
- 1x eMMC NAND-Flash 5.1
- 1x QSPI-NOR-Flash (optional)
- Clock supply
- EEPROM (optional)
- Real-Time-Clock (optional)
- Secure Element Chip (optional)
- Temperature sensor + EEPROM
- Supervisor
- Power Supply

3.1.3 Pin multiplexing

The pin multiplexing of the AM64x / AM243x permits to use many pins for different interfaces.
The information provided in this User's Manual is based on the BSP provided by TQ-Systems GmbH.

Attention: Destruction or malfunction	
	Many AM64x, AM243x pins can be configured as different function. Please take note of the information in the AM64x / AM243x data sheets (1) (2) concerning the configuration of these pins before integration / start-up of your carrier board / Starterkit. Please also take note of the latest AM64x, AM243x errata (4).

3.2 System components

3.2.1 Processor derivatives

Depending on the TQMaX4XxL version, one of the following AM64x/AM243x derivatives is assembled:

- AM6442 / AM6441 / AM6422 / AM6421 / AM6412 / AM6411
- AM2434 / AM2432 / AM2431

Table 2: AM64x derivatives (Source: Texas Instruments)

FEATURES	REFERENCE NAME	AM6442	AM6441	AM6422	AM6421	AM6412	AM6411
Features							
CTRLMMR_WKUP_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit field value[2]		D: 0x19464 E: 0x19465 F: 0x19466	D: 0x19264 E: 0x19265 F: 0x19266	C: 0x19423	D: 0x19224 E: 0x19225 F: 0x19226	C: 0x19403	C: 0x19203
PROCESSORS AND ACCELERATORS							
Speed Grades		See Table 7-1					
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Dual Core	Single Core	Dual Core	Single Core	Dual Core	Single Core
Arm Cortex-R5F	Arm R5F	2 x Dual Core	2 x Dual Core	1 x Dual Core	1 x Dual Core	Single Core	Single Core
Arm Cortex-M4F	Arm M4F	Single Core					
Device Management Security Controller	DMSC-L	Yes					
Cryto Accelerators	Security	Yes					
MCU domain with Arm Cortex-M4F	Safety	Yes					
PROGRAM AND DATA STORAGE							
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	2MB					
R5F Tightly Coupled Memory (TCM)	TCM	256KB	256KB	256KB	256KB	128KB	128KB
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB					
DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 2GB (16-bit data) with inline ECC					
General-Purpose Memory Controller	GPMC	Up to 1GB with ECC					
PERIPHERALS							
Modular Controller Area Network Interface	MCAN	2					
Full CAN-FD Support[3]	MCAN	Optional	Optional	No	Optional	No	No
General-Purpose I/O	GPIO	Up to 198					
Inter-Integrated Circuit Interface	I2C	6					
Analog-to-Digital Converter	ADC	1					
Multichannel Serial Peripheral Interface	MCSPI	7					
Multi-Media Card/ Secure Digital Interface	MMCSD0	eMMC (8-bits)					
	MMCSD1	SD/SDIO (4-bits)					
Fast Serial Interface	FSI_TX	2					
	FSI_RX	6					
Flash Subsystem (FSS)	OSPI0/QSPI0	Yes[1]					
PCI Express Port with Integrated PHY	PCIE0	Single Lane					
Programmable Real-Time Unit Subsystem[4]	PRU_ICSSG	2					
Industrial Communication Subsystem Support[5]	PRU_ICSSG	Optional	Optional	No	Optional	No	No
Gigabit Ethernet Interface	CPSW3G	Yes					
General-Purpose Timers	TIMER	16 (4 in MCU Channel)					
Enhanced Pulse-Width Modulator Module	EPWM	9					
Enhanced Capture Module	ECAP	3					
Enhanced Quadrature Encoder Pulse Module	EQEP	3					
Universal Asynchronous Receiver and Transmitter	UART	9					
Universal Serial Bus (USB3.1 Gen1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY	USB0	Yes					

Table 3: AM243x derivatives (Source: Texas Instruments)

FEATURES(1)	REFERENCE NAME	AM2434 (ALV)	AM2432 (ALV)	AM2431 (ALV)
JTAG DEVICE ID Comparison (Features)				
CTRLMMR_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit-field value(2)		C: ---------- D: 0x19064 E: 0x19065 F: 0x19066	C: 0x19023 D: 0x19024 E: 0x19025 F: 0x19026	C: 0x19003 D: 0x19004 E: ---------- F: ----------
PROCESSORS AND ACCELERATORS				
Speed Grades		See Tal		
Arm Cortex-R5F Processor	R5FSS	2 × Dual Core Cluster	2 × Single Core Cluster	1 × Single Core Cluster
Arm Cortex-M4F Processor	M4FSS	1 × Single Core		
Device Management Security Controller	DMSC-L	Yes		
Crypto Accelerators	Security	Yes		
Functional Safety-capable MCU Domain with M4FSS	Safety	Yes		
PROGRAM AND DATA STORAGE				
Shared On-Chip Memory (OCSRAM) in MAIN Domain	OCSRAM	2MB		
R5F Tightly Coupled Memory (TCM)(3)	TCM	256KB	256KB	128KB
Shared On-Chip Memory (OCSRAM) in MCU Domain	MCU_MSRAM	256KB		
DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 2GB (16-bit data) with inline ECC		
General-Purpose Memory Controller w/Error Location Module (ELM)	GPMC w/ELM	Up to 1GB with ECC		
PERIPHERALS				
Modular Controller Area Network Interface	MCAN	2		
Full CAN-FD Support	MCAN	Optional		
General-Purpose I/O	GPIO	Up to 198		
Inter-Integrated Circuit Interface	I2C	6 (2 in MCU Domain)		
Analog-to-Digital Converter	ADC	1		
Multichannel Serial Peripheral Interface	MCSPI	7 (2 in MCU Domain)		
MultiMedia Card/ Secure Digital Interface	MMC0	eMMC (8-bits)		
	MMC1	SD/SDIO (4-bits)		
Fast Serial Interface	FSI_TX	2		
	FSI_RX	6		
Flash Subsystem (FSS)	OSPI/QSPI	Yes(4)		
PCI Express Port with Integrated PHY	PCIE	Single Lane		
Programmable Real-Time Unit Subsystem (PRU Cores, eGPIO, UART, ECAP. EPWM)	PRU_ICSSG	2		
Industrial Communication Subsystem Support (RGMII/MII and additional Networking Interfaces)	PRU_ICSSG	Optional		
Gigabit Ethernet Interface	CPSW3G	Yes (2 External Ports)		
General-Purpose Timers	TIMER	16 (4 in MCU Domain)		
Enhanced Pulse-Width Modulation Module	EPWM	9		
Enhanced Capture Module	ECAP	3		
Enhanced Quadrature Encoder Pulse Module	EQEP	3		
Universal Asynchronous Receiver/ Transmitter	UART	9 (2 in MCU Domain)		
Universal Serial Bus (USB3.1 Gen1) SuperSpeed Dual-Role-Device (DRD) Port with SS PHY	USB	Yes		

Attention: Malfunction	
	Please take note of the latest AM64x/AM243x errata (4).

3.2.2 Booting

3.2.2.1 Boot source

The boot source is selected via the boot strapping pins of the AM64x / AM243x. The signals are directly routed to the LGA balls and will be available again as GPIO after reading the boot configuration.

After the release of MCU_PORz the boot configuration is read in at the BOOTMODE[15:0] pins. Independent of the boot device, the ROM bootloader is executed first, which assists in reading and executing the application code. The data can be read and loaded either directly from the memory device or by a peripheral.

The following figure shows the implementation of boot strapping on the module:

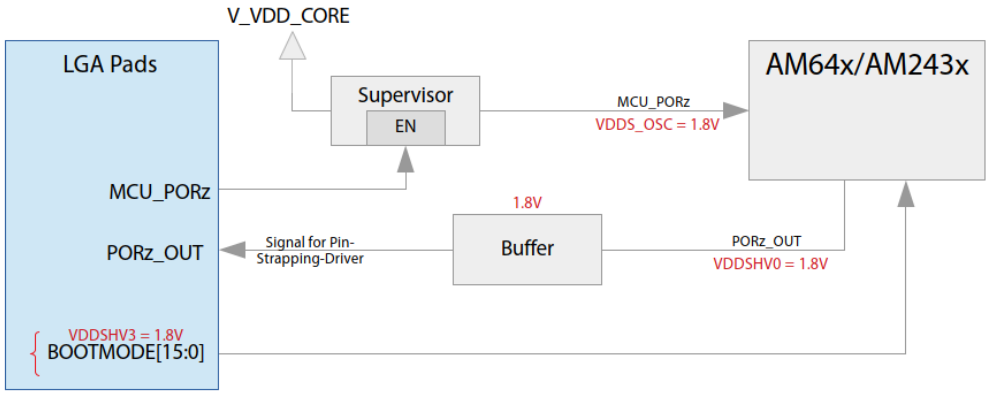

Figure 4: Block diagram Boot-Strapping

According to the Reference Manual (3) the general boot configuration at the TQMaX4XxL can be set as follows:

Table 4: Selecting the General Boot Configuration

Boot configuration pin	Setting	TQMaX4XxL
BOOTMODE[15:14]	Reserved, fixed to 0	00
BOOTMODE[13:10]	Select the backup boot mode, if primary boot device failed	Don't care
BOOTMODE[9:3]	See following chapters for boot devices	-
BOOTMODE[2:0]	Ref Clock Select: 000 = 19.2 MHz 001 = 20 MHz 010 = 24 MHz 011 = 25 MHz 100 = 26 MHz 101 = 27 MHz 110 = Reserved 111 = Reserved	011

Attention: Malfunction	
	All BOOTMODE[15:00] signals must have either a pullup (to V_1V8) or pulldown (to Ground). Undefined levels can lead to a malfunction during booting.

3.2.2.2 Boot device eMMC

Table 5: Boot device selection eMMC

Boot configuration pin	Setting	TQMaX4XxL
BOOTMODE[9]	Port: MMCSD Port 0 (8 bit width) This bit must be set to 0	000
BOOTMODE[8]	Reserved	
BOOTMODE[7]	0 = Filesystem Mode 1 = Raw Mode	
BOOTMODE[6:3]	Primary Boot Mode: 0000 = Reserved 0001 = OSPI 0010 = QSPI 0011 = SPI 0100 = Ethernet RGMII 0101 = Ethernet RMII 0110 = I2C 0111 = UART 1000 = MMCSD boot 1001 = eMMC 1010 = USB 1011 = GPMC NAND 1100 = GPMC NOR 1101 = PCIe 1110 = xSPI 1111 = No-boot/Dev boot	1000

3.2.2.3 Boot device NOR-flash

Table 6: Selection of the boot device NOR flash

Boot configuration pin	Setting	TQMaX4XxL
BOOTMODE9	Reserved, fixed to 0	Don't Care
BOOTMODE8	Clock Source: 0 = Iclock source external 1 = Iclock source internal (pad loopback)	1
BOOTMODE7	Chip-Select: 0 = Boot-Flash is on CS0 1 = Boot-Flash is on CS1	0
BOOTMODE[6:3]	Primary Boot Mode: 0000 = Reserved 0001 = OSPI 0010 = QSPI 0011 = SPI 0100 = Ethernet RGMII 0101 = Ethernet RMII 0110 = I2C 0111 = UART 1000 = MMCSD card 1001 = eMMC 1010 = USB 1011 = GPMC NAND 1100 = GPMC NOR 1101 = PCIe 1110 = xSPI 1111 = No-boot/Dev boot	0011

Further boot configurations can be found in the Reference Manual (3).

Note: Update	
	When designing a mainboard, it is recommended to plan a redundant update concept for software updates in the field. Furthermore, it is recommended to switch the conversion of the boot strap pins to high impedance after reading in.

3.2.3 Memory

3.2.3.1 LPDDR4 SDRAM

The TQMaX4XxL has an LPDDR4 memory with the use of in-line ECC:

- 16-bit bus width with optional ECC (8-bit data + 8-bit ECC)
- Up to 1600 Mbps = 800 MHz

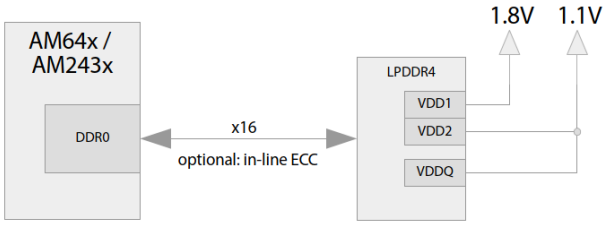

Figure 5: Block diagram DDR3L SDRAM connection

3.2.3.2 eMMC

An eMMC is available to the TQMaX4XxL as non-volatile data memory for programs and data (e.g. boot loader, operating system). The used MMC0 signals are not available to the Pinout.

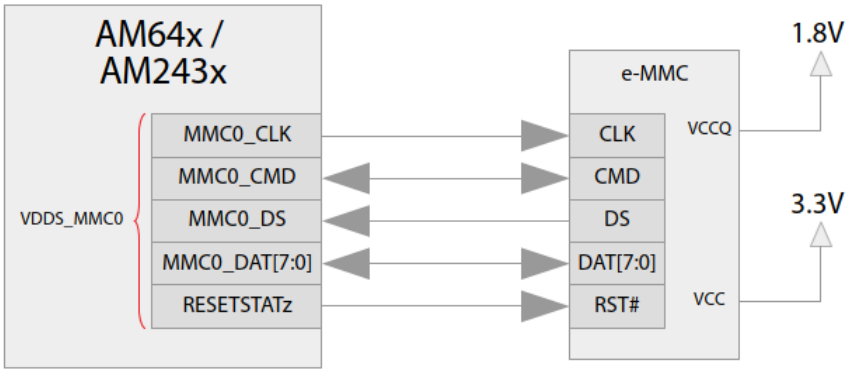

Figure 6: Block diagram eMMC flash interface

The TQMaX4XxL supports the following transmission modes:

Table 7: eMMC Flash modes

Mode	1-bit	4-bit	8-bit	Note
Default Speed	n/a	n/a	n/a	
High Speed	n/a	n/a	X	Boot process
HS200	n/a	n/a	X	U-boot / Linux
HS400	n/a	n/a	n/a	MMCSD not supported features

3.2.3.3 NOR-Flash

A NOR flash is available on the TQMaX4XxL as additional non-volatile memory. The used OSPI0 signals are not available to the pinout.

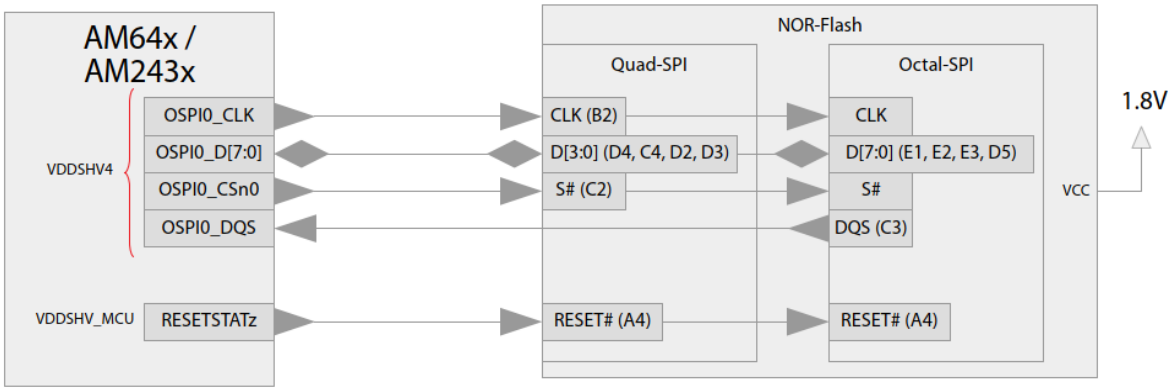

Figure 7: Block diagram NOR-Flash

The NOR-Flash variants Quad SPI Flash and Octal SPI Flash are usable. The TQMaX4XxL supports the following transmission modes:

Table 8: NOR-Flash modes

Mode	Read	Write	Note
Extended SPI (SDR)	1-4-4	1-4-4	Clock = max. 83.33 MHz

3.2.3.4 EEPROMs

I²C EEPROMs are provided on the TQMaX4XxL for non-volatile storage. A distinction is made here between:

- Customer data, freely accessible
- TQ manufacturing data (Serial Number, MAC, ...), not accessible

All I²C slave address and bus structure are summarized in chapter 3.2.8.7.

3.2.4 Clock supply

The clock supply of the TQMaX4XxL is represented as follows:

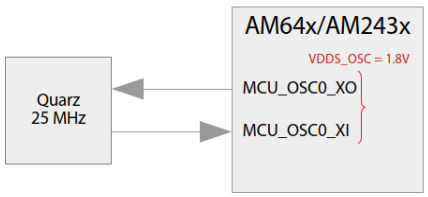

Figure 8: Block diagram clock supply

To get the module executable only with a 5V supply, MCU_OSC0_XO / XI was implemented as clock on the module. The remaining clock inputs can either be derived from the system clock or fed externally via the LGA balls, as an example the following clocks can be fed externally:

- SERDES0_REFCLK0P/N (SerDes Reference Clock)
- MCU_EXT_REFCLK0/1 (optional external System Clock inputs)

Further information can be obtained from the associated data sheets (1) (2).

3.2.5 RTC

An optional RTC (NXP PCF85063A) can be equipped on the TQMaX4XxL. The connection is realized as follows:

- The RTC can be supplied from the base board via V_RTC_IN. V_RTC_IN = 2.0 V to 5.5V
- RTC_INT# and RTC_CLKOUT is accessible at the LGA pads.
- RTC_CLKOUT is only activated as soon as the TQMaX4XxL is supplied with V_5V_IN.
- I2C is connected via I2C0 (I^2C addresses are described in chapter 3.2.8.7)

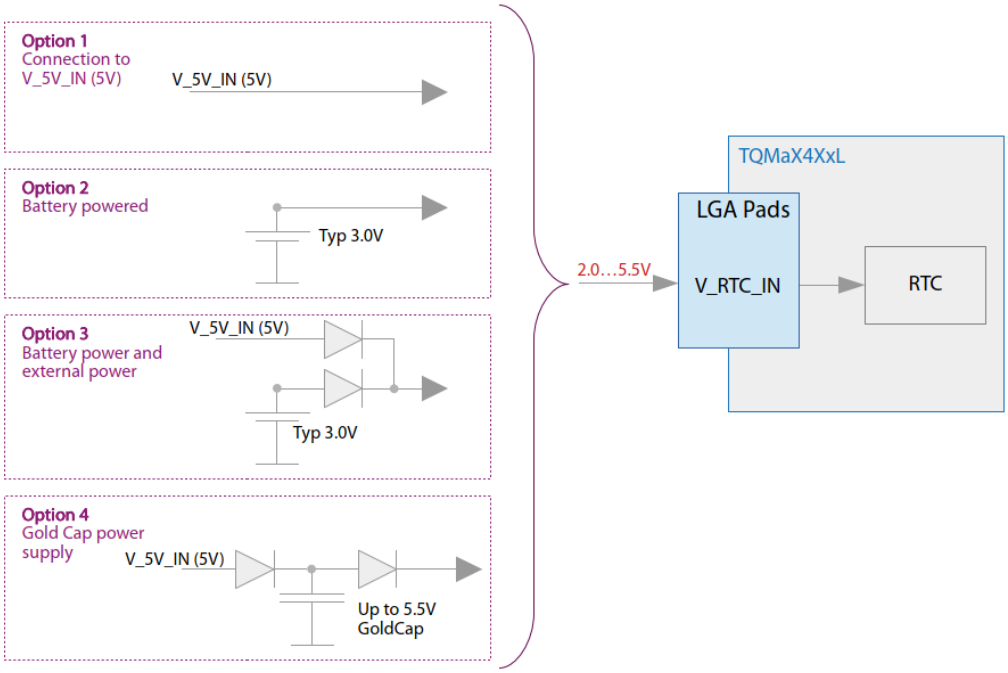

Figure 9: Block diagram RTC

Note: Equipping the base board	
	The RTC is supplied internally by a LDO (1.8V) via V_RTC_IN. This allows the user an easy use of Gold-Caps or Coin cells on the main board.

3.2.6 Secure Element

A Secure Element Chip can optionally be fitted on the TQMaX4XxL. The connection can be seen in the following figure:

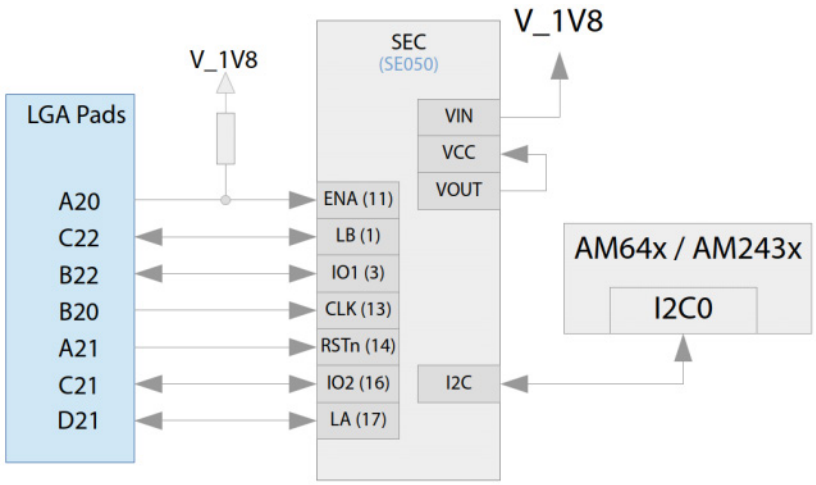

Figure 10: Block diagram SEC

The SE050C2HQ1/Z01 from NXP is used as the secure element. All I²C addresses are described in chapter 3.2.8.7.

3.2.7 Temperature sensor

A temperature sensor (TI TMP1075DSGR) is placed on the TQMaX4XxL to monitor the module temperature.
The over temperature output (TEMP_ALERT) of the sensor is available at the LGA balls as an open drain output.
The I²C addresses are described in chapter 3.2.8.7.

3.2.8 Interfaces

In general, except for the memory connection, all IO pins of the CPU are provided at the LGA pads.
For further information about the interfaces and the pin multiplexing refer to the CPU Reference Manual (3).

3.2.8.1 Ethernet switch

The AM64x / AM243x provides an integrated Ethernet switch (CPSW3G) supporting:

- Up to 2 Ethernet ports
  - RMII (10/100)
  - RGMII (10/100/1000)
- IEEE 1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
- Clause 45 MDIO PHY management
- Energy efficient Ethernet (802.3az)

CPSW3G MDIO0, CPSW3G RMII1, CPSW3G RMII2, and CPSW3G RGMII1 have one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for these interfaces are shown in the AM64x / AM243x data sheets (1) (2).

3.2.8.2 PRU_ICSSG

The Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU_ICSSG) of the AM64x / AM243x provides flexible industrial communications capability including full protocol stacks for EtherCAT slave, PROFINET device, EtherNet/IP adapter, and IO-Link Master. The PRU-ICSSG further provides capability for gigabit and TSN based protocols. In addition, the PRU-ICSSG also enables additional interfaces in the SoC including sigma delta decimation filters and absolute encoder interfaces.

The signals of the PRUs are available as multiplexing options at the pads of the TQMaX4XxL. The IO logic of the interface is 1.8 V.

3.2.8.3 GPIO

Besides their interface function, most AM64x / AM243x pins can also be used as GPIOs. Details are to be taken from the AM64x / AM243x Data Sheet (1) (2).

3.2.8.4 JTAG

The CPU has a JTAG interface that is directly accessible at the LGA pads. The following default configuration is provided on the TQMaX4XxL:

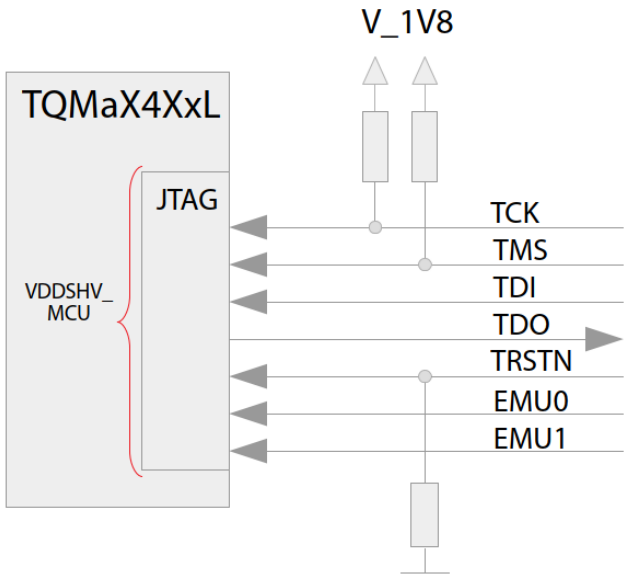

Figure 11: Block diagram JTAG

The following table shows the signals used by the JTAG interface.

Table 9: JTAG signals

Signal / Multiplexing	I/O	Power domain	Note
TCK	I	VDDSHV_MCU (1,8 V)	4.7 kΩ Pull-up on module
TDI	I		
TDO	O		
TMS	I		4.7 kΩ Pull-up on module
TRST#	I		4.7 kΩ Pull-up on module
EMU[1:0]	IO		Optional signals, not required for JTAG

3.2.8.5 SerDes

The CPU has a SerDes lane, which can be used either as PCIe or USB3.0. The signals are directly accessible at the LGA pads. For more information please refer to the Reference Manual (3).

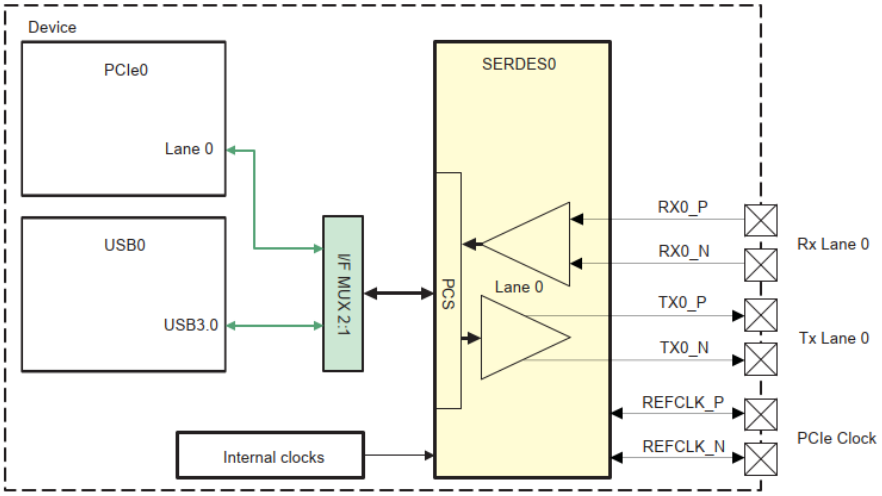

Figure 12: Block diagram SerDes

(Source: Texas Instruments)

3.2.8.6 Serial interfaces

The supported standards, transfer modes and rates of the following interfaces are to be taken from the AM64x / AM243x Data Sheet (1) (2).

3.2.8.7 I²C

The accessible I²C buses depend on the pin multiplexing. To use the internal I²C devices, the I2C0 bus is permanently provided on the TQMaX4XxL. The following devices are connected to the module:

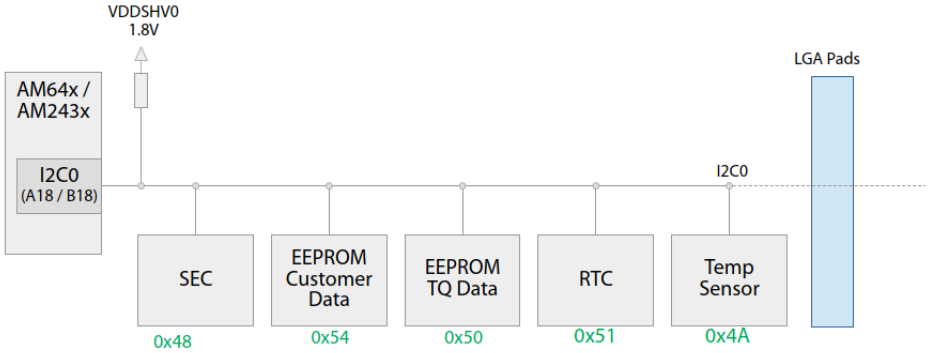

Figure 13: Block diagram I2C bus on the TQMaX4XxL

Die folgende Tabelle zeigt die verwendeten Adressen aller I2C-Busse:

Table 10: I2C address assignment on the module

Bus	Component	Address	Note
I2C0	Temperature sensor TMP1075	0x4A / 0b100 1010	
	EEPROM M24C02	0x50 / 0b101 0000	TQ-Data
	EEPROM M24C64	0x54 / 0b101 0100	Customer EEPROM
	RTC PCF85063ATL	0x51 / 0b101 0001	
	SEC	0x48 / 0b100 1000	

If additional devices should be connected to this bus, optional external pullups should be provided to improve the rise / fall times. I2C0 relates to 1.8V.

3.2.8.8 UART

The TQMaX4XxL provides up to seven UART interfaces. UART0 and UART1 are routed to the TQMaX4XxL pads as primary functions with handshake signals.

3.2.8.9 CAN

The AM64x / AM243x provides up to two integrated CAN controller. The signals of both CAN controller are routed to the TQMaX4XxL pads as primary function. Full CAN-FD support depends on the CPU version.

3.2.8.10 USB

The AM64x / AM243x provides a USB 3.1 port with the signals routed to the TQMaX4XxLpads as primary function. But USB3.1 and PCIe share common SerDes lanes, therefore the functionality is not always available.

In addition the AM64x / AM243x offers a non-shared USB 2.0 routed to the TQM AM64x / AM243x pads (USB0).

3.2.8.11 EXTINT#

The signal EXTINT# of the AM64x / AM243x is routed to TQMaX4XxL pad W17 as primary function.

3.2.9 Reset

The following figure describes the implementation of the reset structure of the TQMaX4XxL:

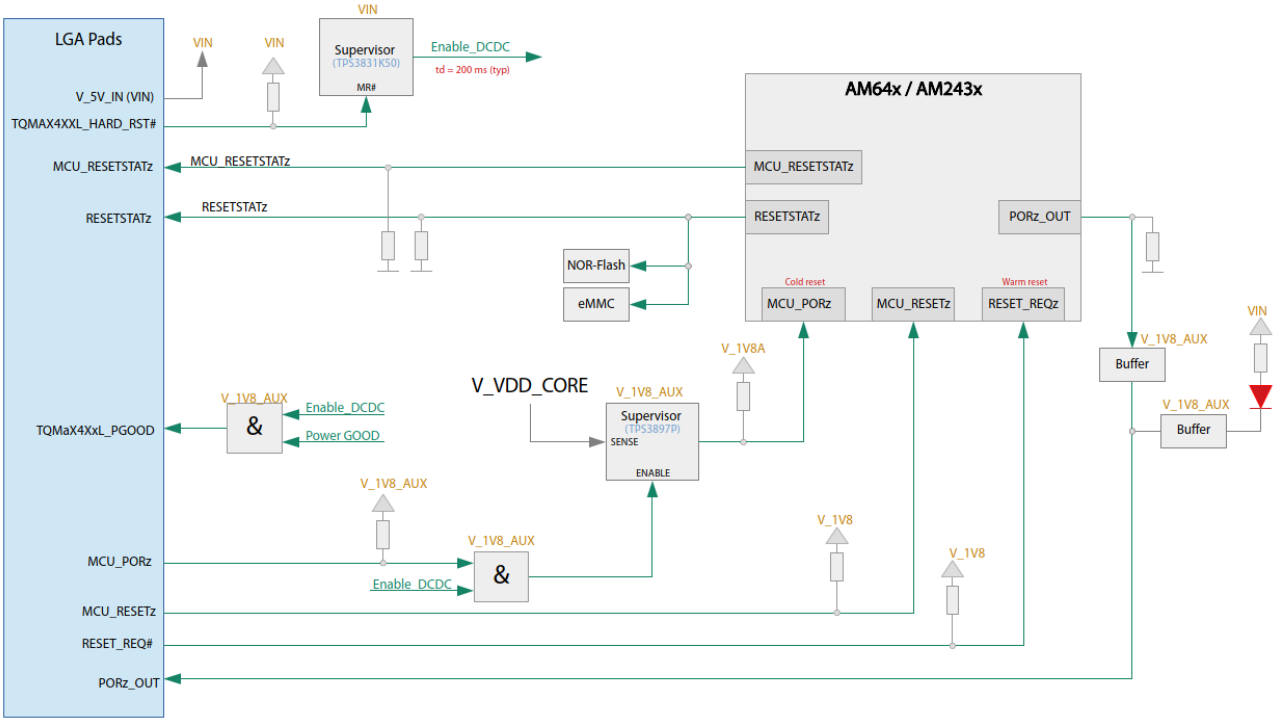

Figure 14: Block diagram Reset

3.2.9.1 Reset Options (Input)

3.2.9.1.1 TQMaX4XxL_HARD_RST#

The input signal TQMaX4XxL_HARD_RST# is used to control the entire module. Coming from the LGA balls a reset with power cycle of the module is executed. As soon as the signal becomes HIGH, the power-up sequencing takes place after a delay of approx. 200 ms.

Per default the signal is connected with a pullup to V_5V_IN (5.0V), therefore only a LOW can reset the module with power cycle.

3.2.9.1.2 MCU_PORz

The MCU_PORz signal is used to control a cold reset. Between the LGA balls MCU_PORz and the AM64x / AM243x MCU_PORz signal is an AND element and a supervisor, which keeps the signal at LOW during power sequencing and pulls it HIGH afterwards.

By default the signal is connected with a pullup to 1.8V, so only a LOW can trigger a cold reset of the module.

3.2.9.1.3 MCU_RESETz

The MCU_RESETz signal is used to control a warm reset of the MCU domain of the AM64x / AM243x.

By default the signal is connected to a pullup to 1.8V, so only a LOW can trigger a warm reset of the MCU domain on the module.

3.2.9.1.4 RESET_REQz

The RESET_REQz signal is used to control a warm reset of the main domain of the AM64x / AM243x.

By default the signal is connected to a pullup to 1.8V, so only a LOW can trigger a warm reset of the main domain on the module.

3.2.9.2 Reset Status (Output)

3.2.9.2.1 PORz_OUT

The PORz_OUT signal serves as status signal for a cold reset of the main domain of the AM64x / AM243x.

By default the signal is driven via a buffer with 1.8V.

3.2.9.2.2 MCU_RESETSTATz

The MCU_RESETSTATz signal serves as a status signal for a warm reset of the MCU domain.

By default the signal is connected with a pulldown to ground.

3.2.9.2.3 RESETSTATz

The RESETSTATz signal serves as a status signal for a warm reset of the main domain.

By default the signal is connected with a pulldown to ground.

3.2.9.2.4 TQMaX4XxL_PGOOD

TQMaX4XxL_PGOOD serves as a status signal to the base board that the voltages on the main board can now be switched on. Power GOOD (PGOOD) is only active when the power sequencing on the module has been successfully completed.

3.2.10 Watchdog

The AM64x / AM243x provides a Watchdog Timer. If the Watchdog-Timer is active and not reset within the specified time, triggers a Warm-Reset. For more information, refer to the AM64x / AM243x Reference Manual (3).

3.2.11 Power supply

3.2.11.1 Main power supply

The main supply of the TQMaX4XxL is defined to typ. 5V. By applying the 5V voltage the module generates all required voltages.

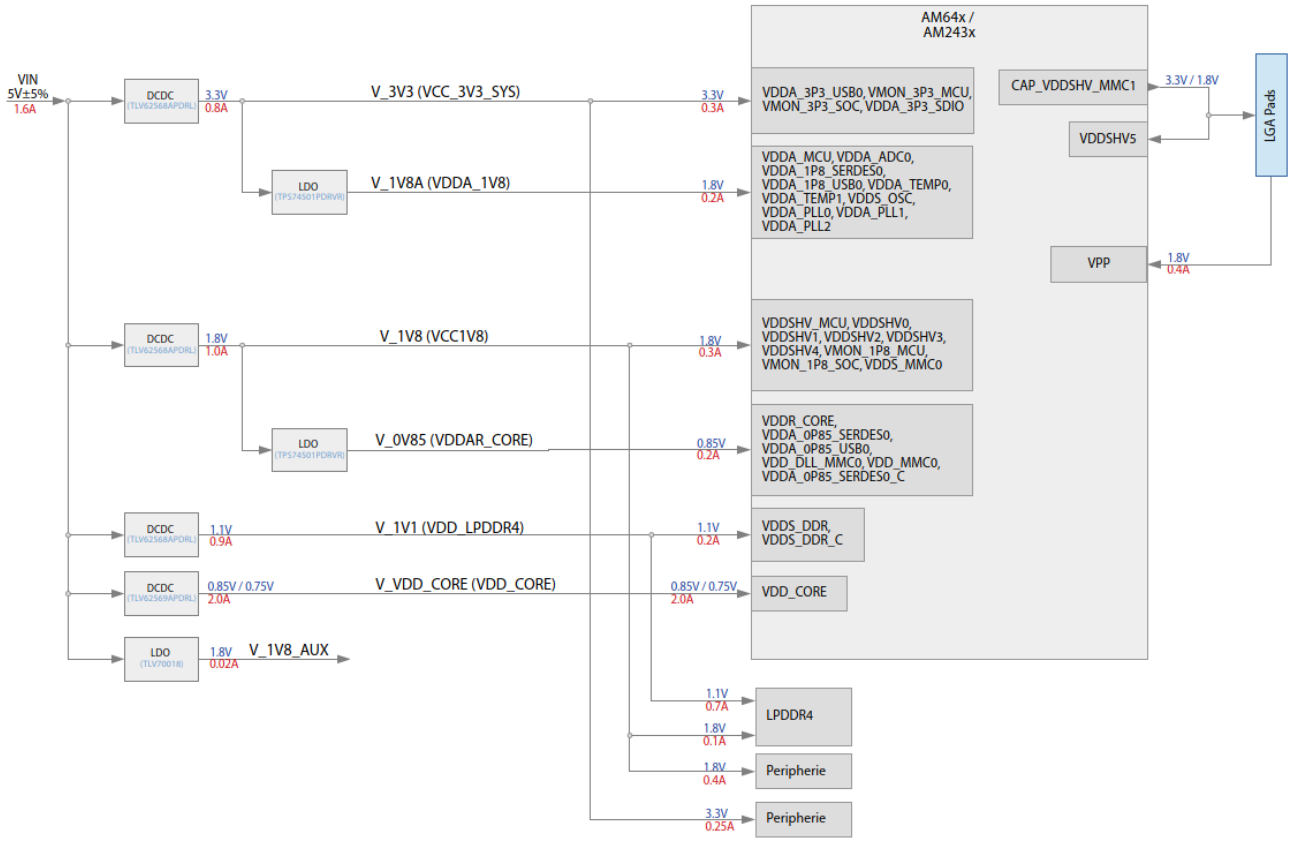

Figure 15: Block diagram power supply

3.2.11.2 Overview TQMaX4XxL supply

The following table shows all relevant supply voltages of the TQMaX4XxL.

Table 11: Supply voltages

Module pin / Signal	Voltage	Current	Use
V_5V_IN	4.75 V to 5.25 V	refer to 3.2.11.5	Input: module supply
V_3V3	3.28 V to 3.36 V	max. 100 mA	Output
V_1V8	1.78 V to 1.82 V	max. 100 mA	Output: for boot configuration
V_VDDSHV5	1.8 V / 3.3 V(3)	< 10 mA	Output: MMC1 IO-bank supply
V_RTC_IN	1.8 V to 5.5 V	refer to 3.2.5	Input: supply for module RTC
V_VPP	1.8 V	max. 400 mA	Input: supply for eFuse programming
USB0_VBUS	typ. 5 V	< 1 mA	Input: Used to detect the USB-VBUS voltage and is usually supplied with the VBUS voltage switched by the USB host. External circuitry is required (3).

Attention: Malfunction	
	If the absolute maximum voltages of the CPU are exceeded, malfunctions and component failures may occur. The mentioned outputs may not be supplied externally under any circumstances.

3.2.11.3 Power sequenzing

After switching on the module supply V_5V_IN and TQMaX4XxL_HARD_RST# to HIGH, the power-up sequence starts. At the end of the power-up sequence, TQMaX4XxL_PGOOD signals the power supply of the external mainboard components. The following figure shows the time sequence of the signal involved:

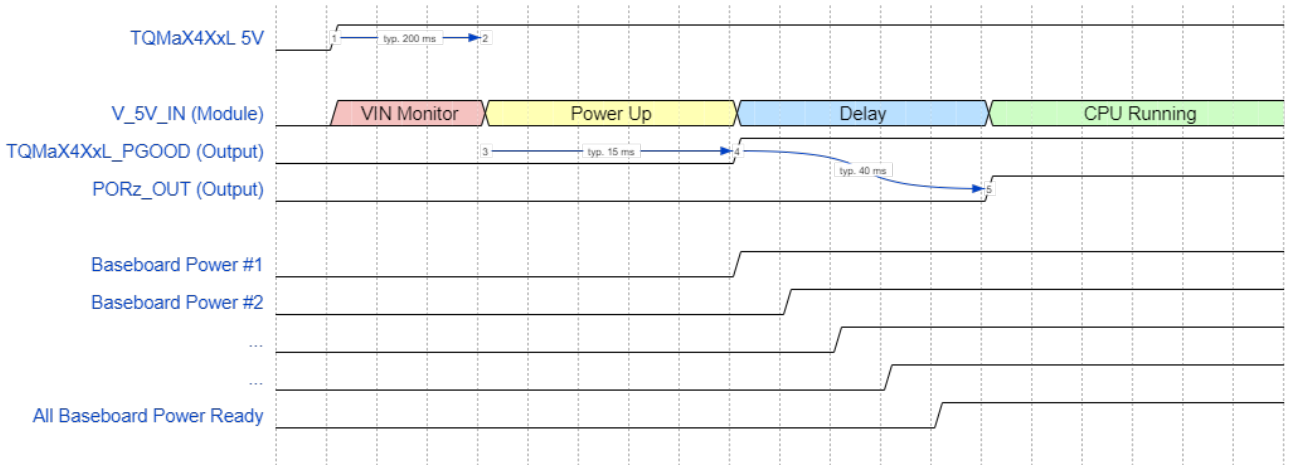

Figure 16: Recommended power up sequence

Attention: Malfunction	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence is completed. The end of the power-up sequence is signaled by a high level of the TQMaX4XxL_PGOOD signal.

3.2.11.4 Power modes

The TQMaX4XxL has the following power modes:

- Active Mode - the module is powered and everything is active.
- Standby Mode - main processor cores in WFI/WFE mode, the rest in idle.

More information can be found in the AM64x / AM243x Reference Manual (3)

Independent of the CPU, the following low power modes can still be provided:

- Module RTC Mode
  - Module is no longer supplied via V_5V_IN
  - Only the V_RTC_IN remains supplied and active
  - The current consumption is then only determined by the current consumption of the RTC
- Self-Refresh Mode (Suspend to RAM)
  - The LPDDR4 memory can be put into self-refresh mode by an SRE command
  - IDD6 is specified in self refresh, typ. current consumption at 25 °C ambient temperature is approx. 0.4 mA to 2.7 mA

3.2.11.5 Power consumption

The following table lists some technical parameters of the module power supply. The specified current consumption values are to be regarded as reference values. Since the power consumption of the TQMaX4XxL can vary greatly depending on the application, mode and operating system, the values listed here should only be used as a performance estimate.

Table 12: Current consumption TQMaX4XxL

TQMa6442L		
Current consumption Reset	7 mA	TQMaX4XxL_HARD_RST# = LOW
Current consumption theoretical worst case	1.6 A	Current consumption @ 4.75V
Current consumption U-Boot prompt	216 mA	U-Boot Idle
Current consumption Linux prompt	255 mA	Linux Idle
Current consumption (stressapptest -W -s 31536000 -M 256 -m 4 -C 4 -i 4 stress-ng --cpu-load 100 --cpu 4 --timeout 31536000)	305 mA	Higher current consumption must be expected when using additional interfaces in parallel

3.3 TQMaX4XxL interface

The TQMaX4XxL has a total of 366 connections, designed as LGA balls, to ensure a high-quality connection when reflow soldering the TQMaX4XxL. By using the LGA design, the module is soldered once and thus has a permanent connection to its periphery. Removing the module from its soldered position is not possible without further ado, is not recommended and can lead to a reduction in the service life or to its destruction.r LGA pads must be free of grease and contamination.

3.3.1 Pin assignment

The multiple pin configurations of all AM64x/AM243x internal function units must be taken note of.

The pin assignment shown in Table 31 refers to the corresponding BSP provided by TQ-Systems GmbH.

The electrical and pin characteristics are to be taken from the AM64x / AM243x (1) (2) (3).

3.3.2 Pinout TQMaX4XxL

The following table shows the pad-out as top view through the TQMaX4XxL.

Table 13: Pinout TQMaX4XxL, top view through TQMaX4XxL

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
22		SE_ISO 7816 _IO1	SE_ISO 14443 _LB	GND	MCU_ SPI0 _CLK	MCU_ SPI0 _D0	GND	MCU_ SPI1 _CLK	MCU_ SPI1 _D0	GND	V_RTC _IN	V_ VPP	GND	RTC_ CLK OUT	RESET STATz	GND	SPI0 _CLK	SPI1 _CLK	GND	ADC0_ AIN6	ADC0 _AIN5		22
21	SE_ISO 7816 _RST#	GND	SE_ISO 7816 _IO2	SE_ISO 14443 _LA	GND	MCU_ SPI0 _D1	MCU_ SPI1 _CS0	GND	MCU_ SPI1 _D1	V_1V8	GND	GND	V_3V3	RTC_ INT#	GND	SPI0 _D0	SPI0 _CS0	GND	SPI1 _CS0	ADC0 _AIN7	GND	ADC0 _AIN4	21
20	SE_ ENA	SE_ISO 7816 _CLK	GND	MCU_ SPI0 _CS0	MCU_ SPI0 _CS1	GND	MCU_ SPI1 _CS1	MCU_ I2C0 _SDA	GND	I2C1 _SDA	I2C1 _SCL	I2C0 _SDA	I2C0 _SCL	GND	RESET _REQz	SPI0 _D1	GND	SPI1 _D0	SPI1 _CS1	GND	ADC0 _AIN3	ADC0 _AIN2	20
19	GND	MCU_ UART0 _RXD	MCU_ UART0 _TXD	GND	MCU_ UART0 _CTS#	MCU_ UART0 _RTS#	GND	MCU_ I2C1 _SCL	MCU_ I2C0 _SCL	GND	CUST_ EEPROM _WC#	TEMP_ ALERT	GND	MCU_ RESETz	MCU_ RESET STATz	GND	SPI0 _CS1	SPI1 _D1	GND	V_VDD SHV5	ADC0 _AIN1	GND	19
18	MCU_ UART1 _RXD	GND	MCU_ UART1 _TXD	MCU_ UART1 _CTS#	GND	MCU_ UART1 _RTS#	MCU_ I2C1 _SDA	GND	EMU1	EMU0	TRST#	TDI	TCK	TDO	GND	TMS	V_RTC	GND	EXT_ REF CLK1	MCU_ SAFETY_ ERROR#	GND	ADC0 _AIN0	18
17	UART0 _RXD	UART0 _TXD	GND	UART0 _CTS#	UART0 _RTS#													ECAP0 _IN_AP WM_OUT	EXT INT#	GND	MCAN0 _RX	MCAN0 _TX	17
16	GND	UART1 _RXD	UART1 _TXD	GND	UART1 _RTS#													OSPI0 _LB CLKO	GND	MCAN1 _RX	MCAN1 _TX	GND	16
15	PRG0_ MDIO0 _MDC	GND	PRG0_ MDIO0_ MDIO	UART1 _CTS#	GND													GND	MMC1_ SDCD	MMC1_ CMD	GND	MMC1 _CLK	15
14	PRG0_ PRU0_ GPO0	PRG0_ PRU0_ GPO1	GND	PRG0_ PRU0_ GPO2	PRG0_ PRU0_ GPO3													OSPI0 _CS1#	MMC1_ SDWP	GND	MMC1_ DAT1	MMC1 _DAT0	14
13	GND	PRG0_ PRU0_ GPO4	PRG0_ PRU0_ GPO5	GND	PRG0_ PRU0_ GPO6													OSPI0 _CS2#	GND	MMC1_ DAT3	MMC1_ DAT2	GND	13
12	PRG0_ PRU0_ GPO7	PRG0_ PRU0_ GPO8	GND	PRG0_ PRU0_ GPO9	PRG0_ PRU0_ GPO10													OSPI0 _CS3#	GPMC0 _CS2#	GND	GPMC0 _CS1#	GPMC0 _CS0#	12
11	PRG0_ PRU0_ GPO11	GND	PRG0_ PRU0_ GPO12	PRG0_ PRU0_ GPO13	GND													GND	GPMC0 _CS3#	GPMC0 _ADV# _ALE	GND	GPMC0 _CLK	11
10	GND	PRG0_ PRU0_ GPO14	PRG0_ PRU0_ GPO15	GND	PRG0_ PRU0_ GPO16													GPMC0 _BE0# _CLE	GND	GPMC0 _AD0	GPMC0 _AD1	GND	10
9	PRG0_ PRU0_ GPO17	PRG0_ PRU0_ GPO18	GND	PRG0_ PRU0_ GPO19	PRG0_ PRU1_ GPO0	GND	V_ 1V1	GND							GND	V_ 0V85	GND	GPMC0 _BE1#	GPMC0 _AD2	GND	GPMC0 _AD3	GPMC0 _AD4	9
8	PRG0_ PRU1_ GPO1	GND	PRG0_ PRU1_ GPO2	PRG0_ PRU1_ GPO3	GND	MCU_ PORz	V_ 1V8 AUX	GND							GND	V_ 1V8A	GPMC0 _DIR	GND	GPMC0 _AD5	GPMC0 _AD6	GND	GPMC0 _AD7	8
7	GND	PRG0_ PRU1_ GPO4	PRG0_ PRU1_ GPO5	GND	PRG0_ PRU1_ GPO6	PORz _OUT	GND	RFU2							RFU3	GND	GPMC0 _WP#	GPMC0 _OE# _RE#	GND	GPMC0 _AD8	GPMC0 _AD9	GND	7
6	PRG0_ PRU1_ GPO7	PRG0_ PRU1_ GPO8	GND	PRG0_ PRU1_ GPO9	PRG0_ PRU1_ GPO10	GND	RFU1	V_VDD _CORE	GND	TQM aX4XxL _HARD _RST#	GND	GND	TQM aX4XxL _PGOOD	GND	TQ_EE PROM _WC#	RFU4	GND	GPMC0 _WE#	GPMC0 _AD10	GND	GPMC0 _AD11	GPMC0 _AD12	6
5	PRG0_ PRU1_ GPO11	GND	PRG0_ PRU1_ GPO12	PRG0_ PRU1_ GPO13	GND	PRG1_ PRU0_ GPO1	PRG1_ PRU0_ GPO4	GND	PRG1_ PRU0_ GPO11	PRG1_ PRU0_ GPO14	PRG1_ PRU0_ GPO18	PRG1_ PRU1_ GPO2	PRG1_ PRU1_ GPO5	PRG1_ PRU1_ GPO9	GND	PRG1_ PRU1_ GPO15	GPMC0 _WAIT0	GND	GPMC0 _AD13	GPMC0 _AD14	GND	GPMC0 _AD15	5
4	GND	PRG0_ PRU1_ GPO14	PRG0_ PRU1_ GPO15	GND	GND	PRG1_ PRU0_ GPO0	GND	PRG1_ PRU0_ GPO7	PRG1_ PRU0_ GPO10	GND	PRG1_ PRU0_ GPO17	PRG1_ PRU1_ GPO1	GND	PRG1_ PRU1_ GPO8	PRG1_ PRU1_ GPO12	GND	PRG1_ PRU1_ GPO18	GPMC0 _WAIT1	GND	USB0 _ID	USB0_ DRV VBUS	GND	4
3	PRG0_ PRU1_ GPO16	PRG0_ PRU1_ GPO17	GND	PRG0_ PRU1_ GPO18	GND	GND	PRG1_ PRU0_ GPO3	PRG1_ PRU0_ GPO6	GND	PRG1_ PRU0_ GPO13	PRG1_ PRU0_ GPO16	PRG1_ PRU1_ GPO0	PRG1_ PRU1_ GPO4	GND	PRG1_ PRU1_ GPO11	PRG1_ PRU1_ GPO14	GND	SERDES 0_REF CLK0_N	SERDES 0_REF CLK0_P	GND	USB0_ VBUS	USB0 _DM	3
2	PRG0_ PRU1_ GPO19	GND	V_5V _IN	V_5V _IN	GND	PRG1_ MDIO0 _MDIO	PRG1_ PRU0_ GPO2	GND	PRG1_ PRU0_ GPO9	PRG1_ PRU0_ GPO12	GND	GND	PRG1_ PRU1_ GPO3	PRG1_ PRU1_ GPO7	GND	PRG1_ PRU1_ GPO13	PRG1_ PRU1_ GPO17	GND	SERDES 0_RX_N	SER DES0 _RX_P	GND	USB0 _DP	2
1		V_5V _IN	V_5V _IN	V_5V _IN	GND	PRG1_ MDIO0 _MDC	GND	PRG1_ PRU0_ GPO5	PRG1_ PRU0_ GPO8	GND	PRG1_ PRU0_ GPO15	PRG1_ PRU0_ GPO19	GND	PRG1_ PRU1_ GPO6	PRG1_ PRU1_ GPO10	GND	PRG1_ PRU1_ GPO16	PRG1_ PRU1_ GPO19	GND	SER DES0 _TX_N	SER DES0 _TX_P		1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	

- TQMaX4XxL -
Top view - through PCB

No pads at corner position A1, A22, AB1 and AB 22

No pads at center position F10 to F17, G10 to G17, H10 to H17, J7 to J17, K7 to K17, L7 to L17, M7 to M17, N7 to N17, P7 to P17, R10 to R17, T10 to T17 and U10 to U17

3.3.2 Pinout TQMaX4XxL (continued)

Table 14: TQMaX4XxL pad description

Module Pad	Signal	CPU Ball	IO	Group	Description	Voltage Level
B1, C1, C2, D1, D2	V_5V_IN	-	P	Input Power Supply	Module Main Power supply Add some blocking capacitors for heavy load transients (typ. 47…100µF)	5.0 V ± 5%
L22	V_RTC_IN	-	P		RTC Power supply	2.0 V to 5.5 V
M22	V_VPP	G15	P		When not pro-gramming OTP registers supply must be disabled. Leave unconnected	1.8 V
K21	V_1V8	-	O	Output Power Supply	V_1V8 power supply Max. 100 mA Should be used for Boot-Strapping	1.8 V ± 5%
N21	V_3V3	-	O		V_3V3 power supply Max. 100 mA	3.3 V ± 5%
Y19	V_VDDSHV5	K15, L14, L15	O		V_VDDSHV5 power supply Max. 20 mA	1.8 V / 3.3 V
K6	TQMaX4XxL_HARD_RST#	-	I	System Signal	Hard Reset to TQMaX4XxL including Power Cycle 10kΩ Pullup on TQMaX4XxL	5.0 V ± 5%
F8	MCU_PORz	-	I		Cold reset to CPU via MCU_PORz 10kΩ Pullup on TQMaX4XxL	1.8 V
P19	MCU_RESETz	B12	I		MCU Domain warm reset 10kΩ Pullup on TQMaX4XxL	
R20	RESET_REQz	E18	I		Main Domain warm reset 10kΩ Pullup on TQMaX4XxL	
F7	PORz_OUT	-	O		Main Domain POR status 10kΩ Pulldown on TQMaX4XxL	
R19	MCU_RESETSTATz	B13	O		MCU Domain warm reset status	
R22	RESETSTATz	F16	O		Main Domain warm reset status	
N6	TQMaX4XxL_PGOOD	-	O		TQMaX4XxL PGOOD Status	
Y18	MCU_SAFETY_ERROR#	A20	IO		Error signal output from MCU Do-main	
L18	TRST#	D11	I	Debug	JTAG Interface TCK, TMS: 4.7kΩ Pullup on TQMaX4XxL TRST#: 4.7kΩ Pulldown on TQMaX4XxL	1.8 V
M18	TDI	C11	I			
T18	TMS	C12	I			
N18	TCK	B11	I			
P18	TDO	A12	O			
K18	EMU0	D10	IO			
J18	EMU1	E10	IO			
	MCU_OBSCLKK0		O			
G6	RFU1	-	-		Reserved for future use Do not connect	-
H7	RFU2	-	-			
R7	RFU3	-	-			
T6	RFU4	-	-			
R6	TQ_EEPROM_WC#	-	I	Factory Test Only	Factory Test only Do not connect	1.8 V
T9	V_0V85	-	P			0.85 V
G8	V_1V8_AUX	-	P			1.8 V
U18	V_RTC	-	P			1.8 V
G9	V_1V1	-	P			1.1 V
H6	V_VDD_CORE	-	P			0.75 V/ 0.85 V
T8	V_1V8A	-	P			1.8 V

3.3.2 Pinout TQMaX4XxL (continued)

Table 32: TQMaX4XxL pad description (continued)

P21	RTC_INT#	-	O	I2C Devices	RTC Interrupt, Open-Drain. Pullup required (typ. 10kΩ)	1.8 V / 3.3V
P22	RTC_CLK_OUT	-	O		RTC Clock Output	1.8 V
M19	TEMP_ALERT	-	O		Programmable Alert Output, Open-Drain. Pullup required (typ. 5kΩ)	1.8 V / 3.3 V
L19	CUST_EEPROM_WC#	-	I		Customer EEPROM Write Protection Control	1.8 V
B22	SE_ISO7816_IO1	-	IO			
C21	SE_ISO7816_IO2	-	IO			
B20	SE_ISO7816_CLK	-	I			
A21	SE_ISO7816_RST#	-	I		SEC Interface	1.8 V
D21	SE_ISO14443_LA	-	IO			
C22	SE_ISO14443_LB	-	IO			
A20	SE_ENA	-	I			
Main domain						
AB11	GPMC0_CLK	R17	O	IO Multiplexing Options	Signal balls with a Pad Configuration Register can be configure as GPIO input and internal pulldown other-wise left unconnected	1.8 V
Y10	GPMC0_AD0	T20	IO			
AA10	GPMC0_AD1	U21	IO			
W9	GPMC0_AD2	T18	IO			
AA9	GPMC0_AD3	U20	IO			
AB9	GPMC0_AD4	U18	IO			
W8	GPMC0_AD5	U19	IO			
Y8	GPMC0_AD6	V20	IO			
AB8	GPMC0_AD7	V21	IO			
Y7	GPMC0_AD8	V19	IO			
AA7	GPMC0_AD9	T17	IO			
W6	GPMC0_AD10	R16	IO			
AA6	GPMC0_AD11	W20	IO			
AB6	GPMC0_AD12	W21	IO			
W5	GPMC0_AD13	V18	IO			
Y5	GPMC0_AD14	Y21	IO			
AB5	GPMC0_AD15	Y20	IO			
AB12	GPMC0_CS0#	R19	O			
AA12	GPMC0_CS1#	R20	O			
W12	GPMC0_CS2#	P19	O			
W11	GPMC0_CS3#	R21	O			
Y11	GPMC0_ADV#_ALE	P16	O			
V10	GPMC0_BE0#_CLE	P17	O			
V9	GPMC0_BE1#	T19	O			
U8	GPMC0_DIR	N17	O			
U5	GPMC0_WAIT0	W19	I			
V4	GPMC0_WAIT1	Y18	I			
U7	GPMC0_WP#	N16	O			
V7	GPMC0_OE#_RE#	R18	O			
V6	GPMC0_WE#	T21	O			
U22	SPI0_CLK	D13	IO			
T21	SPI0_D0	A13	O			
T20	SPI0_D1	A14	I			
U21	SPI0_CS0	D12	O			
U19	SPI0_CS1	C13	O			
V22	SPI1_CLK	C14	IO			
V20	SPI1_D0	B15	O			
V19	SPI1_D1	A15	I			
W21	SPI1_CS0	B14	O			
W20	SPI1_CS1	D14	O			
A17	UART0_RXD	D15	I			
B17	UART0_TXD	C16	O			
D17	UART0_CTS#	B16	I			
E17	UART0_RTS#	A16	O			

3.3.2 Pinout TQMaX4XxL (continued)

Table 32: TQMaX4XxL pad description (continued)

B16	UART1_RXD	E15	I			
C16	UART1_TXD	E14	O			
D15	UART1_CTS#	D16	I			
E16	UART1_RTS#	E16	O			
AA17	MCAN0_RX	B17	I			
AB17	MCAN0_TX	A17	O			
Y16	MCAN1_RX	D17	I			
AA16	MCAN1_TX	C17	O			
N20	I2C0_SCL	A18	IO			
M20	I2C0_SDA	B18	IO			
L20	I2C1_SCL	C18	IO			
K20	I2C1_SDA	B19	IO			
V14	OSPI0_CS1#	L18	O			
V13	OSPI0_CS2#	K17	O			
V12	OSPI0_CS3#	L17	O			
V16	OSPI0_LBCLKO	N21	IO			
AB15	MMC1_CLK	L20	O			
Y15	MMC1_CMD	J19	IO			
AB14	MMC1_DAT0	K21	IO			
AA14	MMC1_DAT1	L21	IO			
AA13	MMC1_DAT2	K19	IO			
Y13	MMC1_DAT3	K18	IO			
W15	MMC1_SDCD	D19	I			
W14	MMC1_SDWP	C20	I			
AB18	ADC0_AIN0	G20	I			
AA19	ADC0_AIN1	F20	I			
AB20	ADC0_AIN2	E21	I			
AA20	ADC0_AIN3	D20	I			
AB21	ADC0_AIN4	G21	I			
AA22	ADC0_AIN5	F21	I			
Y22	ADC0_AIN6	F19	I			
Y21	ADC0_AIN7	E20	I			
W17	EXTINT#	C19	I			
V17	ECAP0_IN_APWM_OUT	D18	IO			
W18	EXT_REFCLK1	A19	I			
MCU domain						
J19	MCU_I2C0_SCL	E9	IO	IO Multiplexing Options	Signal balls with a Pad Configuration Register can be configure as GPIO input and internal pulldown other-wise left unconnected	1.8 V
H20	MCU_I2C0_SDA	A10	IO			
H19	MCU_I2C1_SCL	A11	IO			
G18	MCU_I2C1_SDA	B10	IO			
E22	MCU_I2C0_CLK	E6	IO			
F22	MCU_SPI0_D0	E7	O			
F21	MCU_SPI0_D1	B6	I			
D20	MCU_SPI0_CS0	D6	O			
E20	MCU_SPI0_CS1	C6	O			
H22	MCU_SPI0_CLK	D7	IO			
J22	MCU_SPI1_D0	C7	O			
J21	MCU_SPI1_D1	C8	I			
G21	MCU_SPI1_CS0	A7	O			
G20	MCU_SPI1_CS1	B7	O			
B19	MCU_UART0_RXD	A9	I			
C19	MCU_UART0_TXD	A8	O			
E19	MCU_UART0_CTS#	D8	I			
F19	MCU_UART0_RTS#	E8	O			
A18	MCU_UART1_RXD	C9	I			
C18	MCU_UART1_TXD	D9	O			
D18	MCU_UART1_CTS#	B8	I			
F18	MCU_UART1_RTS#	B9	O			

3.3.2 Pinout TQMaX4XxL (continued)

Table 32: TQMaX4XxL pad description (continued)

PRU						
A15	PRG0_MDIO0_MDC	P3	O	IO Multiplexing Options	Signal balls with a Pad Configuration Register can be configure as GPIO input and internal pulldown other-wise left unconnected	1.8 V
C15	PRG0_MDIO0_MDIO	P2	IO			
A14	PRG0_PRU0_GPO0	Y1	O			
B14	PRG0_PRU0_GPO1	R4	O			
D14	PRG0_PRU0_GPO2	U2	O			
E14	PRG0_PRU0_GPO3	V2	O			
B13	PRG0_PRU0_GPO4	AA2	O			
C13	PRG0_PRU0_GPO5	R3	O			
E13	PRG0_PRU0_GPO6	T3	O			
A12	PRG0_PRU0_GPO7	T1	O			
B12	PRG0_PRU0_GPO8	T2	O			
D12	PRG0_PRU0_GPO9	W6	O			
E12	PRG0_PRU0_GPO10	AA5	O			
A11	PRG0_PRU0_GPO11	Y3	O			
C11	PRG0_PRU0_GPO12	AA3	O			
D11	PRG0_PRU0_GPO13	R6	O			
B10	PRG0_PRU0_GPO14	V4	O			
C10	PRG0_PRU0_GPO15	T5	O			
E10	PRG0_PRU0_GPO16	U4	O			
A9	PRG0_PRU0_GPO17	U1	O			
B9	PRG0_PRU0_GPO18	V1	O			
D9	PRG0_PRU0_GPO19	W1	O			
E9	PRG0_PRU1_GPO0	Y2	O			
A8	PRG0_PRU1_GPO1	W2	O			
C8	PRG0_PRU1_GPO2	V3	O			
D8	PRG0_PRU1_GPO3	T4	O			
B7	PRG0_PRU1_GPO4	W3	O			
C7	PRG0_PRU1_GPO5	P4	O			
E7	PRG0_PRU1_GPO6	R5	O			
A6	PRG0_PRU1_GPO7	W5	O			
B6	PRG0_PRU1_GPO8	R1	O			
D6	PRG0_PRU1_GPO9	Y5	O			
E6	PRG0_PRU1_GPO10	V6	O			
A5	PRG0_PRU1_GPO11	W4				
C5	PRG0_PRU1_GPO12	Y4	O			
D5	PRG0_PRU1_GPO13	T6	O			
B4	PRG0_PRU1_GPO14	U6	O			
C4	PRG0_PRU1_GPO15	U5	O			
A3	PRG0_PRU1_GPO16	AA4	O			
B3	PRG0_PRU1_GPO17	V5	O			
D3	PRG0_PRU1_GPO18	P5	O			
A2	PRG0_PRU1_GPO19	R2	O			
F1	PRG1_MDIO0_MDC	Y6	O			
F2	PRG1_MDIO0_MDIO	AA6	IO			
F4	PRG1_PRU0_GPO0	Y7	O			
F5	PRG1_PRU0_GPO1	U8	O			
G2	PRG1_PRU0_GPO2	W8	O			
G3	PRG1_PRU0_GPO3	V8	O			
G5	PRG1_PRU0_GPO4	Y8	O			
H1	PRG1_PRU0_GPO5	V13	O			
H3	PRG1_PRU0_GPO6	AA7	O			
H4	PRG1_PRU0_GPO7	U13	O			
J1	PRG1_PRU0_GPO8	W13	O			
J2	PRG1_PRU0_GPO9	U15	O			
J4	PRG1_PRU0_GPO10	U14	O			
J5	PRG1_PRU0_GPO11	AA8	O			
K2	PRG1_PRU0_GPO12	U9	O			
K3	PRG1_PRU0_GPO13	W9	O			
K5	PRG1_PRU0_GPO14	AA9	O			

3.3.2 Pinout TQMaX4XxL (continued)

Table 32: TQMaX4XxL pad description (continued)

L1	PRG1_PRU0_GPO15	Y9	O			
L3	PRG1_PRU0_GPO16	V9	O			
L4	PRG1_PRU0_GPO17	U7	O			
L5	PRG1_PRU0_GPO18	V7	O			
M1	PRG1_PRU0_GPO19	W7	O			
M3	PRG1_PRU1_GPO0	W11	O			
M4	PRG1_PRU1_GPO1	V11	O			
M5	PRG1_PRU1_GPO2	AA12	O			
N2	PRG1_PRU1_GPO3	Y12	O			
N3	PRG1_PRU1_GPO4	W12	O			
N5	PRG1_PRU1_GPO5	AA13	O			
P1	PRG1_PRU1_GPO6	U11	O			
P2	PRG1_PRU1_GPO7	V15	O			
P4	PRG1_PRU1_GPO8	U12	O			
P5	PRG1_PRU1_GPO9	V14	O			
R1	PRG1_PRU1_GPO10	W14	O			
R3	PRG1_PRU1_GPO11	AA10	O			
R4	PRG1_PRU1_GPO12	V10	O			
T2	PRG1_PRU1_GPO13	U10	O			
T3	PRG1_PRU1_GPO14	AA11	O			
T5	PRG1_PRU1_GPO15	Y11	O			
U1	PRG1_PRU1_GPO16	Y10	O			
U2	PRG1_PRU1_GPO17	AA14	O			
U4	PRG1_PRU1_GPO18	Y13	O			
V1	PRG1_PRU1_GPO19	V12	O			
W3	SERDES0_REFCLK0_P	W17	IO	SERDES Reference Clock In-put/Output	Leave unconnected	-
V3	SERDES0_REFCLK0_N	W16	IO			
Y2	SERDES0_RX_P	Y16	I	SERDES differential Receive Data		
W2	SERDES0_RX_N	Y15	I			
AA1	SERDES0_TX_P	AA17	O	SERDES differential Transmit Data		
Y1	SERDES0_TX_N	AA16	O			
AB2	USB0_DP	AA19	IO	Differential Data Line USB2.0	Float	-
AB3	USB0_DM	AA20	IO			
AA3	USB0_VBUS	T14	I	USB VBUS Detection		max. 3.6 V
Y4	USB0_ID	U16	I	USB Dual-Role Device Role Select		3.3 V
AA4	USB0_DRVVBUS	E19	O	USB VBUS Control Output (active high)		1.8 V
A4, A7, A10, A13, A16, A19, B2, B5, B8, B11, B15, B18, B21, C3, C6, C9, C12, C14, C17, C20, D4, D7, D10, D13, D16, D19, D22, E1, E2, E3, E4, E5, E8, E11, E15, E18, E21, F3, F6, F9, F20, G1, G4, G7, G19, G22, H2, H5, H8, H9, H18, H21, J3, J6, J20, K1, K4, K19, K22, L2, L6, L21, M2, M6, M21, N1, N4, N19, N22, P3, P6, P20, R2, R5, R8, R9, R18, R21, T1, T4, T7, T19, T22, U3, U6, U9, U20, V2, V5, V8, V11, V15, V18, V21, W1, W4, W7, W10, W13, W16, W19, W22, Y3, Y6, Y9, Y12, Y14, Y17, Y20, AA2, AA5, AA8, AA11, AA15, AA18, AA21, AB4, AB7, AB10, AB13, AB16, AB19					Digital Ground	

IO Types:

- I: Input
- O: Output
- IO: Input / Output
- P: Power

4. SOFTWARE

The TQMaX4XxL is shipped with a specially adapted bootloader, which is configured for use on an MBaX4XxL.
This bootloader contains module specific as well as board specific adjustments like e.g.

- CPU configuration
- RAM configuration / timing
- Multiplexing
- Clocks
- Driver strengths

If a different bootloader is used, these data must be adapted. Details can be requested from TQ support. Further information can be found in the Support Wiki for the TQMaX4XxL.

5. MECHANICS

5.1 TQMaX4XxL dimensions and footprint

The overall dimensions (length × width) of the TQMaX4XxL are 38 mm × 38 mm.
The maximum height of the TQMaX4XxL above the carrier board is approximately 4.3 mm.
The mass of TQMaX4XxL is 10 g (± 2 g)

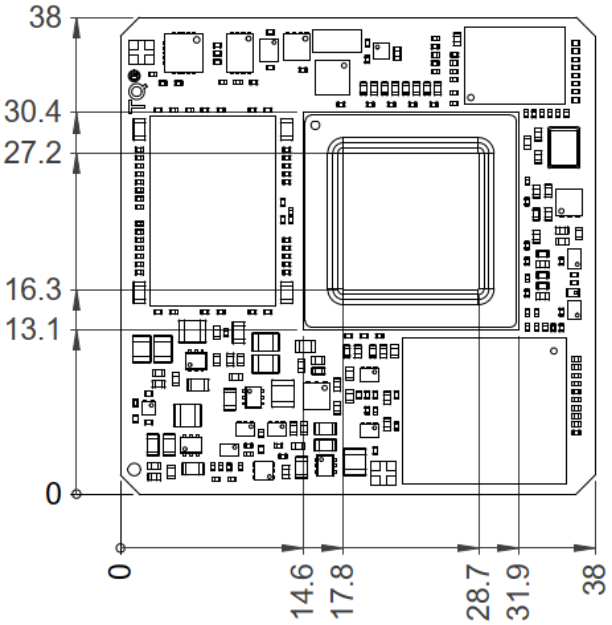

Figure 17: TQMaX4XxL dimensions (1)

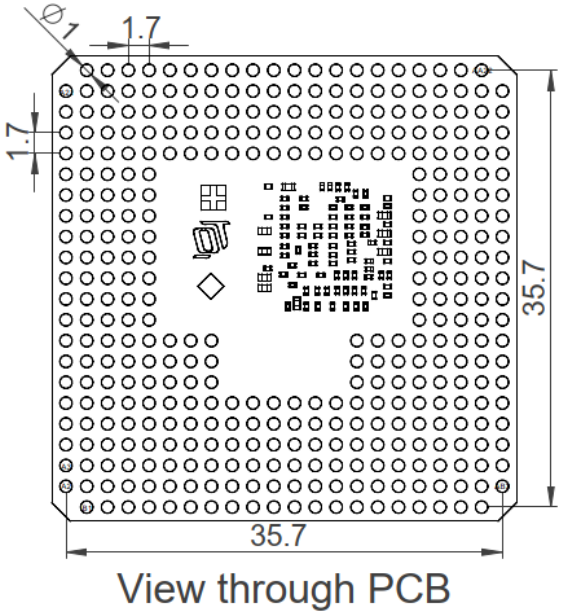

Figure 18: TQMaX4XxL dimensions (2)
Top view through TQMaX4XxL

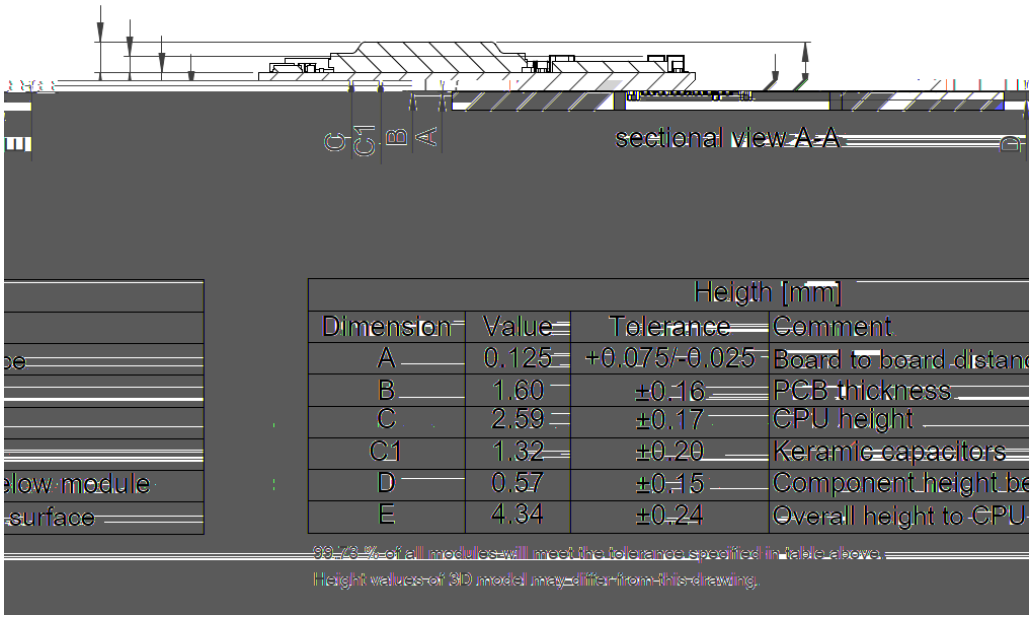

Figure 19: TQMaX4XxL side view

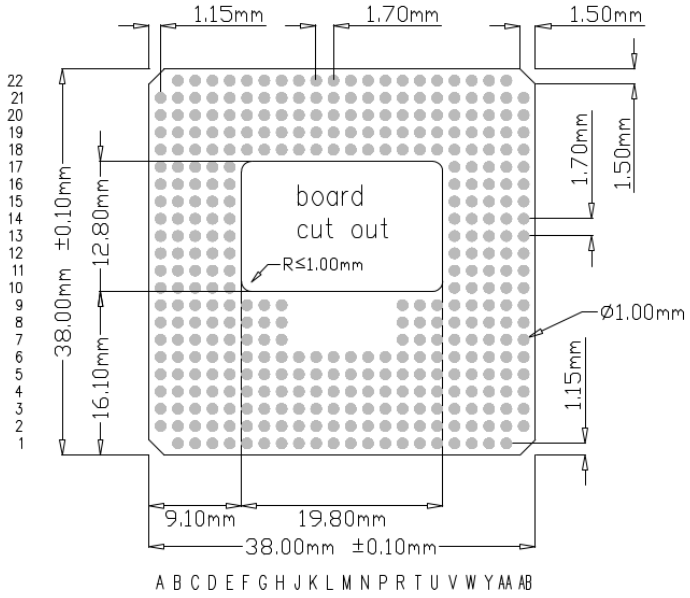

Figure 20: Recommended PCB land pattern for TQMaX4XxL, top view through TQMaX4XxL

5.2 TQMaX4XxL component placement

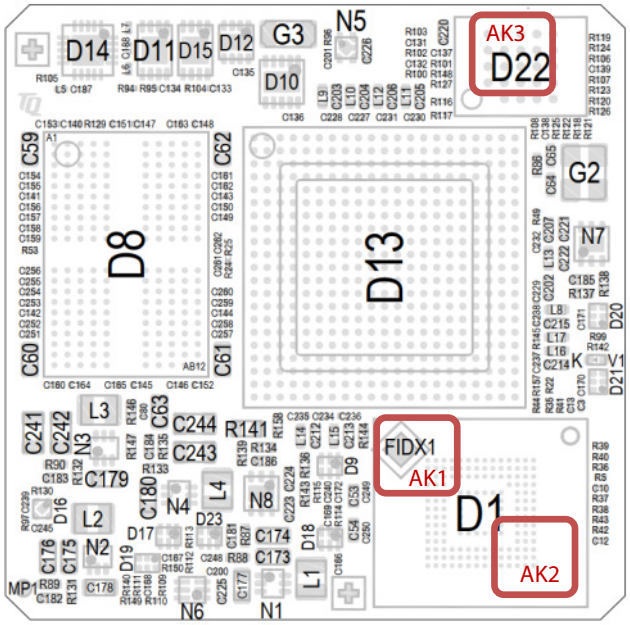

Figure 21: TQMaX4XxL component placement top

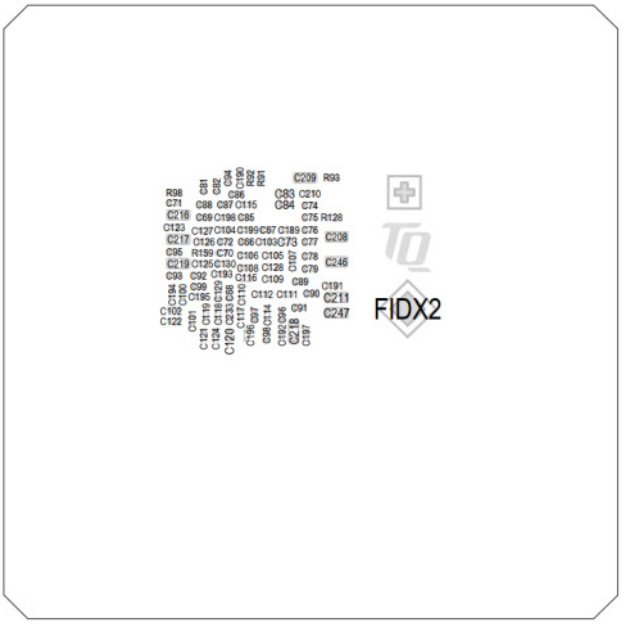

Figure 22: TQMaX4XxL component placement bottom

The labels on the TQMaX4XxL show the following information:

Table 15: Labels on TQMaX4XxL

Label	Text
AK1	TQMaX4XxL 2D serial number
AK2	TQMaX4XxL MAC address
AK3	TQMaX4XxL version and revision

5.3 Protection against external effects

As an embedded module the TQMaX4XxL is not protected against dust, external impact and contact (IP00).

Adequate protection has to be guaranteed by the surrounding system.

5.4 Thermal management

The power dissipation mainly depends on the software used and can vary according to the application. The power dissipation mainly arises at the processor, the switching regulators and the LPDDR4 devices. It is the customer's responsibility to define a suitable cooling method for his use case.

Attention: Destruction or malfunction, TQMaX4XxL cooling	
	The AM64x/243x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM64x/243x must be taken into consideration when connecting the heat sink, see (5). The AM64x/243x is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMaX4XxL and thus malfunction, deterioration or destruction.

5.5 Structural requirements

The TQMaX4XxL has to be soldered on the carrier board. The TQMaX4XxL is held on the mainboard by the holding force of the solder connections from the LGA pads and requires no further fastening measures. If there are high requirements for vibration and shock resistance, a module holder must be provided in the final application to additionally hold the module in position. Since no heavy and large components are used, there are no further requirements.

Attention: Note on equipping the base board	
	To ensure a high-quality connection of the LGA pads when reflow soldering the TQMaX4XxL, the LGA pads must be free of grease and contamination. Please contact TQ-Support for soldering instructions (7).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMaX4XxL was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding besides, take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.
As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMaX4XxL.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety haven't been carried out.

6.4 Intended Use

TQ DEVICES, PRODUCTS AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION IN NUCLEAR FACILITIES, AIRCRAFT OR OTHER TRANSPORTATION NAVIGATION OR COMMUNICATION SYSTEMS, AIR TRAFFIC CONTROL SYSTEMS, LIFE SUPPORT MACHINES, WEAPONS SYSTEMS, OR ANY OTHER EQUIPMENT OR APPLICATION REQUIRING FAIL-SAFE PERFORMANCE OR IN WHICH THE FAILURE OF TQ PRODUCTS COULD LEAD TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE. (COLLECTIVELY, "HIGH RISK APPLICATIONS")

You understand and agree that your use of TQ products or devices as a component in your applications are solely at your own risk. To minimize the risks associated with your products, devices and applications, you should take appropriate operational and design related protective measures.

You are solely responsible for complying with all legal, regulatory, safety and security requirements relating to your products. You are responsible for ensuring that your systems (and any TQ hardware or software components incorporated into your systems or products) comply with all applicable requirements. Unless otherwise explicitly stated in our product related documentation, TQ devices are not designed with fault tolerance capabilities or features and therefore cannot be considered as being designed, manufactured or otherwise set up to be compliant for any implementation or resale as a device in high risk applications. All application and safety information in this document (including application descriptions, suggested safety precautions, recommended TQ products or any other materials) is for reference only. Only trained personnel in a suitable work area are permitted to handle and operate TQ products and devices. Please follow the general IT security guidelines applicable to the country or location in which you intend to use the equipment.

6.5 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.6 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.
The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

6.7 Climatic and operational conditions

The temperature range, in which the TQMaX4XxL works reliably, strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.
In general, a reliable operation is given when following conditions are met:

Table 16: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Environmental temperature	–40 °C to +85 °C	With appropriate cooling
Permitted storage temperature	–40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

6.8 Reliability and service life

For the TQMaX4XxL, a constant error rate results in an MTBF of approximately 1,044,757 hours (TQMa6442) and approximately 1,065,228 hours (TQMa2434).

Attention must be paid to a construction that is insensitive to vibration and shock.

Service life-limiting components such as electrolytic capacitors were not used.

6.9 Environment protection

6.9.1 RoHS

The TQMaX4XxL is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

6.9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMaX4XxL was designed to be recyclable and easy to repair.

6.10 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

6.11 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMaX4XxL must therefore always be seen in conjunction with the complete device.

The available standby and sleep modes of the components on the TQMaX4XxL enable compliance with EuP requirements for the TQMaX4XxL.

6.12 Battery

No batteries are used on the TQMaX4XxL.

6.13 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMaX4XxL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMaX4XxL is delivered in reusable packaging.

6.14 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

6.15 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

7. APPENDIX

7.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 17: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AIN	Analog In
ARM®	Advanced RISC Machine
AVS	Adaptive Voltage Scaling
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
DC	Direct Current
DDR3L	Double Data Rate Type three Low voltage
DIN	Deutsche Industrie Norm
DVS	Dynamic Voltage Scaling
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multi-Media Card
EN	Europäische Norm
ESD	Electro-Static Discharge
EU	European Union
EuP	Energy using Products
FR-4	Flame Retardant 4
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input/Output
GPMC	General Purpose Memory Controller
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IP	Ingress Protection
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MCSPI	Multichannel Serial Port Interface
MD	Management Data
MII	Media-Independent Interface
MMC	Multi-Media Card
MTBF	Mean operating Time Between Failures

7.1 Acronyms and definitions (continued)

Table 43: Acronyms (continued)

Acronym	Meaning
n.a.	Not Available
NC	Not Connected
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PRCM	Power and Clock Management
PU	Pull-Up
PWM	Pulse-Width Modulation
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection
WXGA	Wide Extended Graphics Array

7.2 References

Table 18: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	AM64x Sitara Processors Datasheet	A / June 2021	Texas Instruments
(2)	AM243x Sitara Microcontrollers Datasheet	A / June 2021	Texas Instruments
(3)	AM64x / AM243x Processors Silicon Revision 1.0 Technical Reference Manual	B / June 2021	Texas Instruments
(4)	Errata AM64x/AM243x Processor Silicon Revision	Rev B / June 2021	Texas Instruments
(5)	MBaX4XxL User's Manual	– current –	TQ-Systems
(6)	Support-Wiki for the TQMaX4XxL	– current –	TQ-Systems
(7)	Processing instructions for TQMaX4XxL	– current –	TQ-Systems

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